CHARACTERIZING DEVICE EFFICIENCY POTENTIAL FROM INDUSTRIAL MULTI-CRYSTALLINE CELL STRUCTURES COMPOSED OF SOLAR GRADE SILICON

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ABSTRACT: This comparative study is presented to illustrate several key relationships between impurity density in the silicon wafer and device performance within a baseline silicon nitride firing-through cell process. Results are given as a function of solidification fraction on multi-crystalline production ingots, and link cell investigations to the solar grade silicon (SoG-Si) blends. Illuminated current-voltage characteristics of SoG-Si cells having a compensated, net acceptor concentration up to 3 x 10^{17} cm^{-3} show equivalent conversion efficiencies relative to control cells (η > 15.3%), and excellent open circuit voltage measurements (V_{oc} > 625 mV). As net acceptor concentration is further increased, recombination influences minority carrier lifetime and offsets corresponding increases in open circuit voltage. To identify metallic impurity species responsible for recombination, laser beam induced current and microwave detected photo-conductance decay mappings are combined with elemental analysis from secondary ion mass spectrometry in the phosphorus-gettered region. Upon optimizing diffusion conditions to create a tailored emitter profile, enhanced short circuit current values were obtained (J_{sc} > 32.5 mA cm^{-2}). Infrared luminescence images of reverse biases cells are paired with leakage currents measured during dark current-voltage characterization and expressed as a function of net-ionized dopants. Light induced degradation findings on SoG-Si cells are contrasted with other work and proposed explanations from elemental analysis offered. Near-term performance extensions through advanced cell constructions are explored on full size (η > 16.1%) and on small area devices (η > 17.8%) to illustrate SoG-Si feedstock potential.

KEYWORDS: Metallurgical Solar Grade Silicon, Multicrystalline Silicon Solar Cells, Feedstock Assessment

1 INTRODUCTION

Molten phase refining of metallurgical grade silicon has the potential to augment the material supply of a resource constrained multi-crystalline solar cell industry, given that acceptable purity is attained. Dow Corning, and others [1-3], have introduced solar grade silicon (SoG-Si) feedstock to the market in support of the rapid expansion of cell manufacturing capabilities. Though generally not as pure as electronic grade silicon produced from gas phase impurity separation, comparable solar cell efficiencies have been reported over a range of dopant, metallic, and carbon impurity densities using SoG-Si [4-6]. A primary driver in the cost to produce SoG-Si is the removal rate of boron and phosphorus. Hence the concentrations of each are typically high relative to electronic grade silicon and rely on compensation to deliver wafer resistivity within specifications. This body of work highlights several key relationships between ionized and inactive dopant concentrations that must be considered when increasing SoG-Si impurity density. Further, device processing optimizations used to obtain improved results on these substrates are investigated to assess unrealized potential within an industrially standard architecture.

2 WAFER CHARACTERISTICS

To illustrate trends in increasing the dopant concentration of SoG-Si, six multi-crystalline (mc-Si) ingots were produced having compositions shown in Figure 1. This surveys donor densities (phosphorus) ranging from 1 x 10^{14} cm^{-3} to 5 x 10^{17} cm^{-3} that are compensated by boron to yield net acceptor densities ranging from 1 x 10^{16} cm^{-3} to 3 x 10^{17} cm^{-3}.

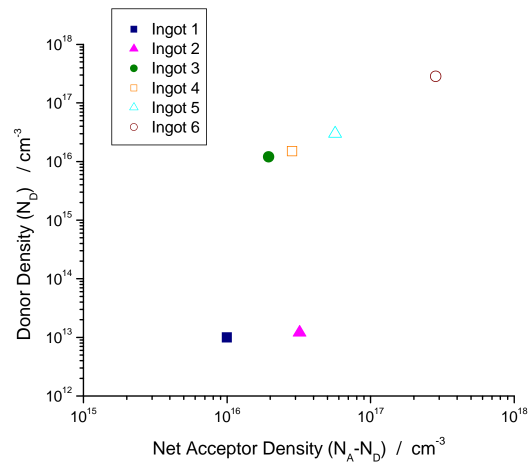

Figure 1: Ingot composition survey range illustrating compensation levels investigated

Each 265 kg charge was subjected to identical crystal growth conditions within a standard gradient freeze furnace. The resulting ingots were sectioned into 150 mm x 150 mm x 220 mm blocks and sliced to 220 µm thick wafers. Laser coding enabled identification of individual wafers within the 16 block pattern. Discrete wafers from corresponding blocks are

chosen to serve as characterization specimens and link solidification fraction and net acceptor density to each result.

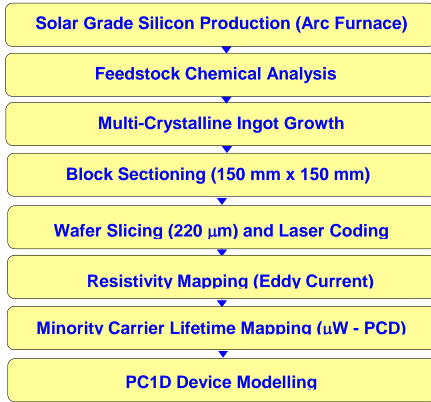

Figure 2: Material preparation and wafer characterization outline

2.1 Dopant Segregation

During directional solidification, impurities partition at the solid-liquid interface in accordance to the additional free energy associated with their incorporation into the silicon lattice. The Scheil a relationship [7,8] shown in Equation 1 is used to determine an impurity profile in the crystal. Equilibrium segregation coefficients (k^{i}_{eq}) 0.8 for boron and 0.35 for phosphorus and initial feedstock concentrations (C^{i}_{o}) are used to determine dopant concentration profile in the crystal (C^{*}_{s}) as a function of solidification fraction (f_s).

$$C_S^* = \kappa C_o (1 - f_S)^{(\kappa - 1)}$$

Equation 1

The net acceptor density, N_A-N_D, is calculated from individual donor and acceptor concentration profiles where the excess acceptor concentration is used to calculate p-type resistivity [9]. This approach is modeled for each ingot in Figure 3.

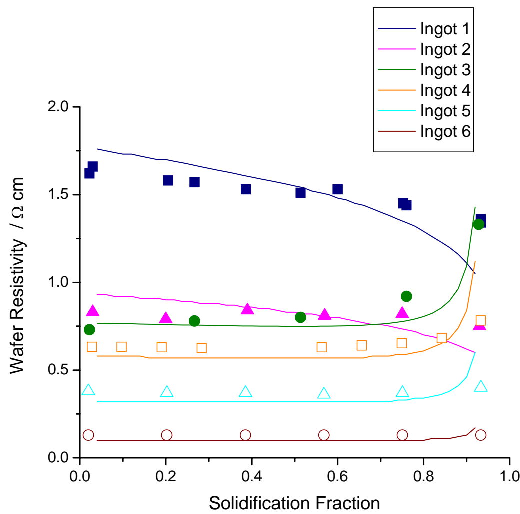

Figure 3: Scheil-based dopant segregation models compared to wafer resistivity

Eddy current resistivity measurements taken on individual wafers are plotted along with predicted resistivity profiles in Figure 3. Wafer resistivity lowers with increasing net acceptor concentration, while the variation through solidification is decreased as compensation increases as in ingots 3-6. Compensated ingots show a sharp increase in resistivity at $f_s > 0.95$ leading to a type transition at $f_s = 0.97$. This finding is congruent with the increasing phosphorus concentration at the top of the ingot.

2.2 Minority Carrier Lifetime

Figure 4 represents as-grown minority carrier lifetimes for select wafers in the central block of each ingot. Measurements using a microwave photo conductance decay instrument employ a SiN_x passivation coating to reduce surface recombination. Therefore the bulk lifetime is assumed [10] to be limited by Auger and Shockley-Read-Hall recombination in accordance with Equation 2 and Equation 3.

$$\frac{1}{\tau_{net}} = \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}}$$

Equation 2

$$\frac{1}{\tau_{Aug}} \alpha \frac{1}{N_A^2}$$

Equation 3

A characteristic mc-Si pattern of lifetime is observed whereby τ_{net} at the base of the ingot is influenced by metal and oxygen contamination from the crucible, a broad maximum in τ_{net} exists throughout a large portion of the block, while the end of solidification retains concentrated metal or carbon concentrations and significantly reduced measured τ_{net} values. Where net acceptor concentrations are high as in Ingot 6, a constant of $\tau_{net} < 7$ μs is seen throughout the entire block.

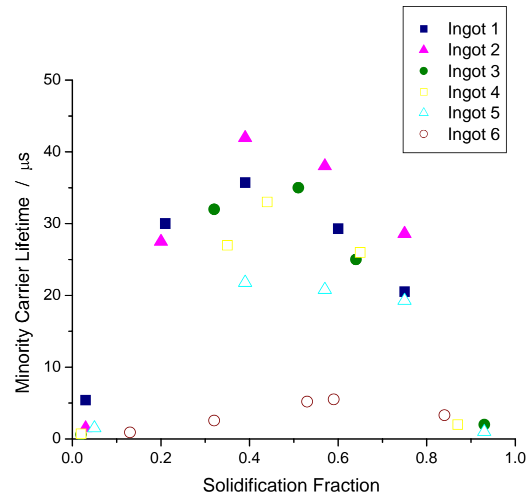

Figure 4: Minority carrier lifetime as a function of solidification fraction for each ingot

In comparing ingot average lifetimes of Figure 5, net acceptor densities near 2 x 10^{16} cm^{-3} appear to provide optimal best results. Interestingly, compensation ingots near this net acceptor density, only have a small reduction from peak lifetimes observed ($\Delta\tau_{net}$= 5-7 μs).

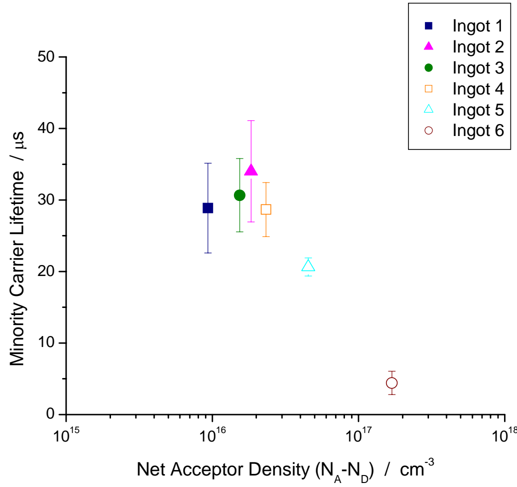

Figure 5: Block average minority carrier lifetime as a function of net acceptor density for each ingot

The effect of compensation on as-grown lifetime has been observed by others [11,12]. This work illustrates that lifetime was observed to increase slightly with moderate levels of compensation. However, subsequent thermal treatments can limit lifetime gains if the emitter diffusion is not properly matched to higher net acceptor densities.

3 SOLAR CELL PROCESSES AND RESULTS

To better understand the impact of resistivity and net acceptor density on a standard solar cell process, PC1D simulations were conducted over a range of substrate thicknesses [13]. From Figure 6, it can be noted that acceptor densities within ingot 4, corresponding to 0.53 Ω cm, predict roughly an increase in $\Delta\eta \approx 0.1\%$ over ingot 1 at 1.5 Ω cm. Further, as slicing technologies enable thinner mc-Si wafers and better surface passivation approaches emerge, device efficiency dependence on τ_{bulk} in the model will be reduced and higher efficiencies become readily achievable.

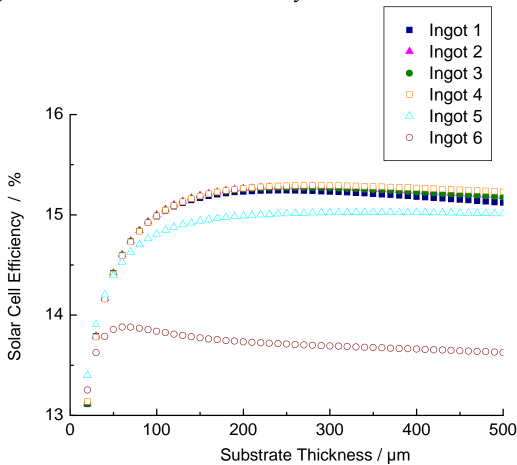

Figure 6: PC1D simulations showing cell efficiency as a function of substrate thickness for various net acceptor densities in a standard device process

3.1 Standard Characterization Devices

A standard industrial p-type process was applied to wafers in the central block of each ingot. Figure 7 depicts a process outline consisting of alkaline saw damage etch, $POCl_3$ gas/glass diffusion to obtain a 40-55 Ω/sq emitter, edge isolation and glass removal conducted via horizontal etching, plasma enhanced CVD of the SiN_x antireflection coating, screen-printed metallization followed by IR lamp belt furnace co-firing. Surface texturing was not conducted in this process to accentuate the differences in device current for each substrate composition.

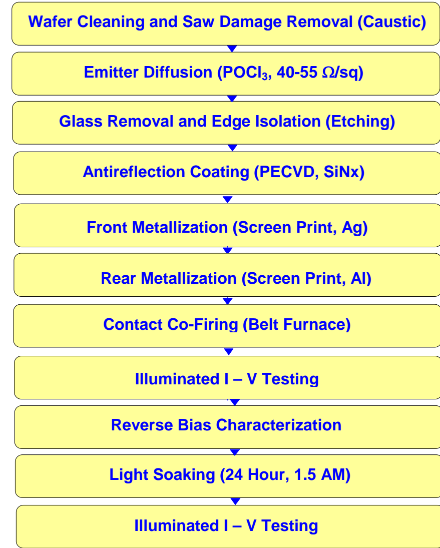

Figure 7: Standard device processing and characterization outline

Illuminated current-voltage data from is located in Figure 8. Note that excellent agreement to simulated cell efficiency of Figure 6 was achieved from this process. Table I summarizes the statistical data. An increasing V_{oc} trend is evident relating net acceptor concentration increases toward a maximum of 625.7 mV for ingot 5 at $6x10^{16}$ cm^{-3}. Also from inspection, the trend in J_{sc} as a function of fraction solidified mimics that of τ_{net}. However, a mean of 32.2 mA cm^{-2} is obtained despite moderate net acceptor concentrations in ingot 4. The combination of higher V_{oc} and comparable J_{sc} contributes to superior device efficiencies for compensated ingot 4 and comparable efficiencies for ingots 3 and 5. It follows that material composing ingot 6 which does not benefit from a high V_{oc} at 0.15 Ω cm resistivity, is limiting efficiency potential within this process.

Table I: Results from industrial cell process

	V_{oc} [mV]		J_{sc} [mA cm^{-2}]		Eta [%]	
	Ave	*Std Dev.*	*Ave*	*Std Dev.*	*Ave*	*Std Dev.*
Ingot 1	614.8	*6.5*	32.1	*0.8*	14.6	*0.6*
Ingot 2	618.5	*5.2*	31.8	*0.9*	14.7	*0.7*
Ingot 3	616.3	*5.9*	30.0	*0.5*	14.3	*0.6*
Ingot 4	622.7	*3.5*	32.2	*0.5*	15.1	*0.4*
Ingot 5	625.9	*1.5*	31.1	*0.3*	14.6	*0.3*
Ingot 6	609.2	*5.0*	27.9	*0.4*	10.6	*0.8*

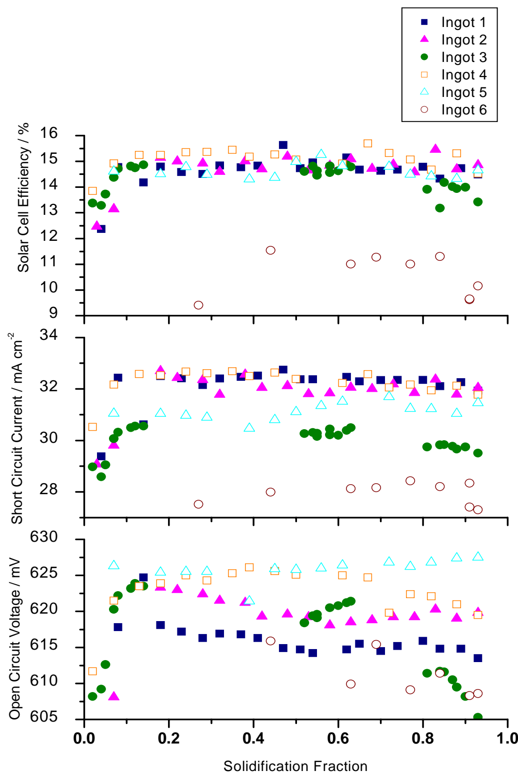

Figure 8: Measured open circuit voltage (bottom), short circuit current (middle), and solar cell efficiency (top) as a function for solidification fraction for each ingot

Characterization of the above cells in reverse bias can identify potential module reliability issues under partially shaded conditions. Therefore, imaging of these cells under reverse bias is done with a thermographic foil adhered to the cell surface as well as infrared luminescence imaging. Both methods can identify localized areas of junction breakthrough. Pictured in Figure 9 is a wafer from Ingot 5 using the two visualization approaches. Under a V_{app} of -24 VDC, the blue regions on the foil indicate high temperature regimes. The lighter sections of the infrared luminescence image indicate these same positions on the cell surface.

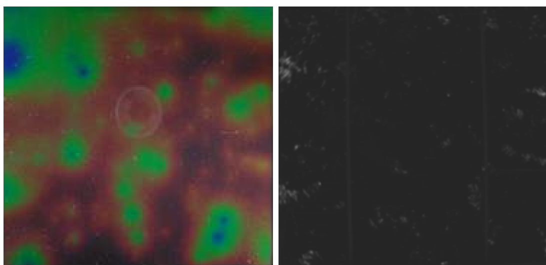

Figure 9: Thermographic foil and infrared luminescence imaging under reverse bias, localized heating indicative of junction break through

Precipitate or inclusion presence have been cited as a possible causes for regions of localized heating [14], SEM, EDX, and SIMS investigations did not confirm the presence of any impurity rich particles. Therefore, it is suspected that breakdown occurs only through avalanche carrier multiplication. The voltage at which this breakdown occurs can be described by the following relationship [10] in Equation 4 and indicative in the trend observed in Figure 10:

$$V_{br} = \frac{\varepsilon_s E_m^2}{2qN}$$

Equation 4

The inverse dependence on acceptor concentration shown in Equation 4 is detected to be the net acceptor concentration through measurements made on these cells. Mean breakdown voltages for ingots 1- 6, show this strong correlation to net acceptor density. This is confirmed by the higher donor concentration of ingot 3 relative to ingot 2, yielding equivalent V_{br} values.

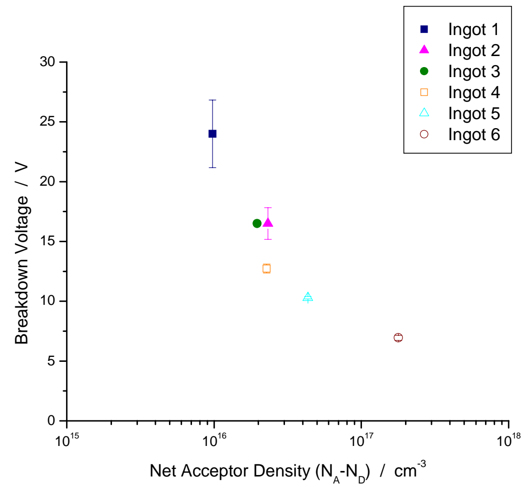

Figure 10: Measured breakdown voltage as a function of net acceptor density for each ingot

Light induced degradation is another module reliability parameter investigated within this survey. Figure 11 illustrates the mean change in V_{oc} after 24 hours of light soaking at AM 1.5.

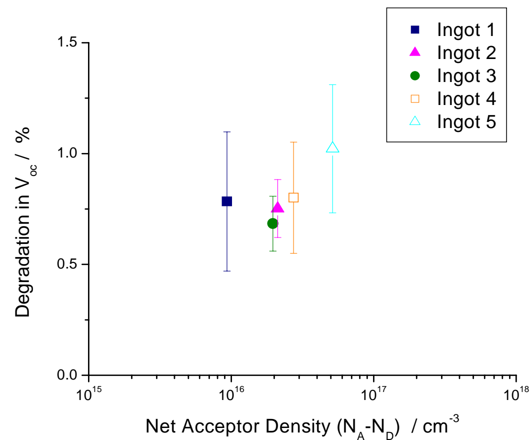

Figure 11: Average change in open circuit voltage as a result of light induced degradation (AM 1.5) after 24 hours

From the measurements, V_{oc} appears to degrade with higher net acceptor concentrations. But at equivalent net acceptor densities as in ingots 2 and 3, identical V_{oc} losses are detected. Light induced degradation in these cells is therefore dependent on the net boron concentration and not total boron concentration. This result is consistent with other work presented by fellow researchers [15]. From this it follows that boron-oxygen defect pairs formation may only be possible on excess boron not effectively compensated by phosphorus. Further investigation into the possibility of the net benefit to using increased donor concentration to mitigate light induced degradation is planned.

4.2 Optimizations for Solar Grade Silicon

Several optimizations within the device process have been undertaken in to maximize the mean efficiency of ingots 1-6 and illustrate the potential of SoG-Si. Figure 12 outlines rationale for specializing several process parameters for application to these unique materials.

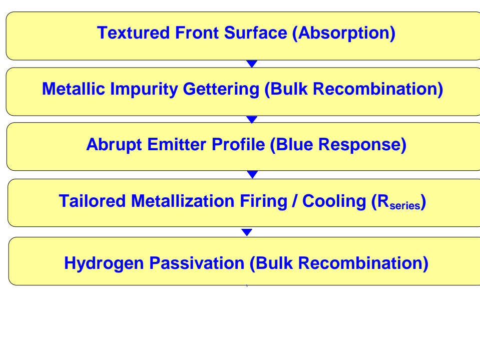

Figure 12: Device optimization outline

Acid texturing was introduced to increase light absorption though it is not directly related to material quality. Increases in photon fluxes should therefore be constant for all cell compositions yielding positive gains in J_{sc} for all cells.

Open tube furnace phosphorus gettering was performed on wafers from each ingot to study the ability to accumulate metals toward the surface of the wafer [16]. Temperatures ranging from 820°C to 1050°C were investigated and results shown in Figure 13. Surface removal of effectively 15 µm per side via acid etching was conducted to remove this contamination layer. Cleaning and passivating of etched surfaces took place before µW-PCD measurements to draw comparisons to as-grown lifetimes. From Figure 13 it can be observed that both ingots benefitted by gettering. However, the increase in mean wafer lifetimes post gettering from ingot 4 continued until temperatures above 950 °C, whereas ingot 1, peaked in lifetime at an annealing temperature of 850 °C.

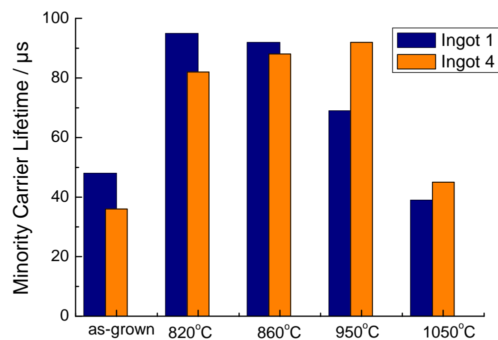

Figure 13: Assessing the optimal sheet resistance for net acceptor density of ingot 4

Junction formation methods for SoG-Si wafers require adjustment from uncompensated wafers. Because a heavily doped emitter is required to offset the net acceptor concentration of the base, the junction depth should be greater for low resistivity wafers. Low acceptor concentration wafers can take advantage of a lightly doped, shallow junction to convert low wave length photons more readily. Solar grade silicon wafers must have high temperature and longer diffusion time to broaden the emitter profile. Figure 14 shows a 55 Ω/sq emitter profile, measured by ECV, before and after optimization to yield an abrupt doping profile.

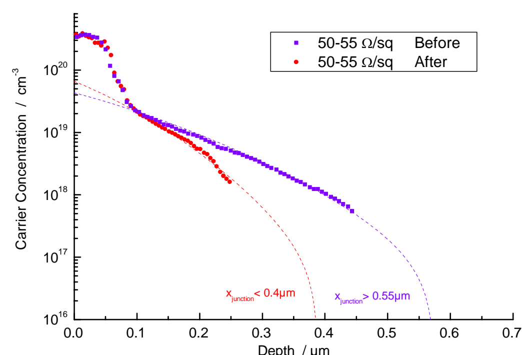

Figure 14: Abrupt emitter profile illustrating equivalent sheet resistance and improved minority carrier lifetime

As was experienced in emitter diffusion, the elevated net acceptor concentrations of ingots 3 – 6 required further process developments to ensure an excellent fill factor, create a strong Al back surface field, and completely passivate remaining bulk defects with hydrogen released from the SiN_x layer. A tailored metallization firing condition toward achieving the lowest series resistance aids fill factor. Cooling rates were altered from the standard cell process to locate the minimum series resistance for these cells. Also, because the net acceptor concentration is high in these substrates, the relative difference between the base resistivity and the p^+ BSF formed by Al alloying is reduced. Carrier extraction can then be optimized through a proper alloying time/temperature profile and Al layer thickness. Finally, increased defects in SoG-Si wafer require additional hydrogen concentration adequately passivate the bulk. PECVD with directed exposure and a hydrogen rich environment will ensure maximum hydrogen

incorporation into the SiN_x:H film. The cell results obtained after these extensions to the standard cell process are given in Table II.

Table II: Results for optimized standard cell process

	V_{oc} [mV]		J_{sc} [mA cm^{-2}]		Eta [%]	
	Ave	Std Dev.	Ave	Std Dev.	Ave	Std Dev.
Ingot 1	611.6	0.7	33.8	0.1	15.8	0.3
Ingot 2	613.0	4.1	32.7	0.2	14.9	0.2
Ingot 3	617.7	1.7	33.3	0.1	15.5	0.2
Ingot 4	620.5	0.7	33.5	0.1	15.8	0.2
Ingot 5	618.2	3.7	31.6	0.1	14.6	0.2
Ingot 6	609.5	7.9	28.9	0.2	11.5	0.9

4.3 High Efficiency Cell Process

To assess the impact of net acceptor concentration on high efficiency devices, a process described in Figure 15 is been applied to ingot 4 wafers. Pre-phosphorus gettered wafers were selected based on high lifetime values, and segmented into 2 cm x 2 cm sections using a dicing saw. Figure 16 shows a spatially resolved lifetime map with selected regions for solar cell processing. Then diffusion of a 100 Ω/sq emitter was followed by PECVD SiN_x deposition. Al metal paste rear contact printing was completed before photolithography patterned and evaporated Ti/Pd/Ag front contacts, which were subsequently galvanized then sintering in a microwave induced remote hydrogen plasma [17]. A FZ wafer of equivalent net acceptor concentration was used as a process reference.

Figure 15: High efficiency device process outline

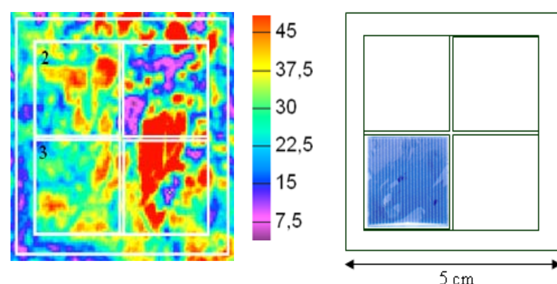

Figure 16: Gettered region for advanced device processing on SoG-Si wafers

Extending the process to achieve better light trapping was conducted by applying a second antireflection layer of MgF_2 to wafers from ingot 4. Results from both efforts are shown in Table III

Table III: Results for high efficiency cell process, single and double antireflection layer (DARL)

	V_{oc} [mV]		J_{sc} [mA cm^{-2}]		Eta [%]	
	Ave	Std Dev.	Ave	Std Dev.	Ave	Std Dev.
FZ-Si Ref	634.5	2.1	33.0	0.1	16.6	0.3
Ingot 4	636.1	0.7	32.3	0.1	16.5	0.1
(DARL) Ingot 4	637.5	0.8	34.6	0.1	17.8	0.1

5 CONCLUSIONS

Six ingots were produced with varying net acceptor density achieved through various levels of compensation. Comparable minority carrier lifetimes were observed on ingots with net acceptor densities less than 3 x 10^{16} cm^{-3}, despite heavy donor concentrations in two ingots. Mean solar cell efficiency of SoG-Si wafers was aided by an increase in V_{oc} due to lower resistivity with equivalent J_{sc} due to minimal recombination in the bulk. Reverse bias measurements indicate a strong correlation of break down voltage with net acceptor density and not the total boron concentration. Also, only the net boron concentration appears to influence V_{oc} losses after light soaking. Optimizations within a standard cell process for SoG-Si wafers have lead to mean efficiencies greater than 15.8% with a best cells having η = 16.1% on industrial-sized substrates. High efficiency cell processing techniques were employed to achieve η= 17.8% on 2 cm x 2 cm cells, showing minimal performance limitations from the feedstock at these compensation levels.

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